

DYNAMIC SLEEP-CONTROLLED PR9T SRAM CELL FOR LOW LEAKAGE AND POWER-BALANCED MEMORY DESIGN

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Abstract: This paper presents the transistor-level implementation, transient functional verification, and supply-current analysis of the PMOS-Reading 9T (PR9T) SRAM cell in 45 nm Cadence Virtuoso technology. The PR9T architecture features a single-ended write path, a power-gated write-support pair, a decoupled PMOS-based read path on the complementary storage node (QB), and a leakage-balancing transistor (MAD) is designed . Transient simulations verify all six SRAM operations: write-1, hold-1, read-1, write-0, hold-0, and read-0. Control-signal waveforms confirm correct synchronization of the write and read paths . These results establish a functional and analytical foundation for leakage-aware SRAM evaluation

Keywords: SRAM, PR9T, PMOS Read Path, Leakage Power Analysis, Cadence Virtuoso, 45 nm CMOS, Write Stability, Static Leakage Current

I. INTRODUCTION

This Static Random Access Memory (SRAM) is a fundamental building block of modern digital systems, widely used in cache memories, register files, and embedded applications. With technology scaling into deep-submicron regimes, low-power and security-aware SRAM design has become increasingly important. Conventional 6T SRAM cells suffer from read disturbance and write difficulty .

The PMOS-Reading 9T (PR9T) SRAM cell addresses these challenges by introducing a decoupled PMOS-based read path , write mechanism, and a leakage-balancing transistor (MAD). These architectural features collectively improve read stability, write robustness, and leakage symmetry between stored data states. The present work implements and verifies the PR9T concept in 45 nm Cadence Virtuoso, providing transistor-level functional validation and quantitative supply-current analysis .

II. Review of Dynamic Sleep-Controlled PR9T SRAM Cell for low Leakage and Power-Balanced Memory Design Architecture

1. **Top-Level Architecture Overview:** The PR9T (PMOS-Reading 9T) SRAM cell is a security-aware, low-power memory cell implemented in 45 nm Cadence Virtuoso with VDD = 1 V. The architecture is divided into four distinct functional blocks operating independently.

2. **Cross-Coupled Storage Latch :** Forms the central memory core using two back-to-back CMOS inverters. Generates complementary nodes Q and QB representing the stored binary state. Regenerative feedback maintains data indefinitely after write access is removed. Directly evaluated through hold-mode stability in transient simulation.

3. **Single-Ended Write Path :** One NMOS access transistor connects WBL to Q, gated by WL. Replaces the dual-bit line scheme of conventional 6T SRAM with a single WBL. Reduces dynamic power and bit line switching activity. Write-0 is faster and stronger than write-1 due to NMOS pull-down characteristics.

4. **Power-Gated Write Support:** WLPU and WLPD transistors temporarily weaken latch feedback during write. Enables reliable data overwrite without permanently degrading hold stability. Switches back to normal hold condition immediately after WL is deasserted.

5. **PMOS-Based Decoupled Read Path :** PMOS read transistor placed on QB side, controlled via VVSS and connected to RBL. PMOS chosen over NMOS for stronger logic-'1' transfer and lower read-branch leakage. Read does not disturb Q or QB, giving high RSNM and non-destructive operation.

6. **MAD Transistor :** Connected near QB branch as a leakage-path modifier, not a switching element. Equalizes off-state leakage current between Q=0 and Q=1 stored states.

7. **Architectural Separation of Write and Read :** The most critical architectural principle of PR9T is the complete isolation of write and read .

Table 2.1 : Write-Read-Hold Mode Control Signal Separation in PR9T SRAM

MODE	ACTIVE SIGNAL	INACTIVE SIGNAL
Write	WL =1, WLPU=1, WLPD=0	VVSS=1 (read off)
Read	VVSS=0	WL = 0 (write off)
Hold	WL=0, VVSS=1	All paths are isolated

8. Architectural Comparison with related cells

Table 2.2: Comparison of SRAM Architecture

Feature	6T	PR9T
Read Port	Shared	PMOS Decoupled
Bit line Scheme	Dual	Single
LPA Resistance	Low	High (MAD)
Transistor Count	6	9

9. Architectural Strengths :

- Write robustness : power-gating ensures reliable data overwrite at scaled nodes.
- Read stability : PMOS decoupled path eliminates read disturbance completely.
- Power efficiency : single-ended bit line lowers active energy vs. 6T.
- Modularity : write and read paths are fully independent and separately controllable.

III. Review of evaluation parameters

The following performance metrics are considered ;

1. RSNM : Decoupled PMOS read path prevents storage node disturbance, significantly improving Read Static Noise Margin over 6T SRAM.
2. Power Consumption Single-ended bit line : It reduces dynamic power and static leakage power
3. Write Robustness Power-gating pair (WLPU/WLPD) : It weakens the latch during write, enabling reliable data overwrite for both logic states.
4. MAD transistor: It balances data-dependent leakage between stored states, reducing exploitable current differences in Leakage Power
5. Hold Stability Cross-coupled latch : This successfully retains both Q=1 and Q=0 states across their respective hold intervals with no node drift.

III. Circuit design and simulation:

1. Overall PR9T Cell Architecture : The implemented PR9T cell consists of three main functional sections: (1) the cross-coupled CMOS latch forming the storage core, (2) the single-ended write path connected through the write bit line (WBL), and (3) the PMOS-based decoupled read path connected through the read bit line (RBL). The cell was designed and simulated in Cadence Virtuoso using 45 nm technology models with a 1 V supply voltage.

2. Cross-Coupled Storage Latch: The storage core is formed by two back-to-back CMOS inverters generating complementary nodes Q and QB. Once

data is written, the cross-coupled feedback preserves the stored state independently of the bit line conditions. The stability of these nodes during hold mode is critical to SRAM functionality.

3. **Single-Ended Write Path** : The write path uses a single NMOS access transistor controlled by the write word line (WL). When WL is asserted, the value present on WBL is transferred to node Q, and QB resolves automatically through the latch. This single-ended scheme reduces dynamic switching activity and active power compared with conventional dual-bit line 6T SRAM. The NMOS access transistor passes logic '0' more strongly than logic '1', resulting in a sharper falling transition at Q during write-0 operations.

4. **Power-Gated Write Support (WLPU / WLPD)** : Two power-gating transistors, controlled by WLPU and WLPD, temporarily modify the latch drive strength during write operations. WLPU rises and WLPD falls during the write interval, weakening the cross-coupled feedback and enabling the incoming write data to overwrite the stored state more effectively.

5. **Leakage-Balancing Transistor (MAD)** : The MAD transistor is a defining feature of the PR9T architecture. Its purpose is to balance the off-state leakage current between the two possible stored states, so that the leakage signature observed at the supply is less data-dependent.

6. **PMOS-Based Decoupled Read Path** : The read path is placed on the QB side and uses a PMOS read transistor controlled via VVSS and the read bit line RBL. PMOS is preferred over NMOS in the read path because it provides stronger logic-1 transfer capability and contributes lower leakage in the read branch. The decoupled structure ensures that the internal storage nodes are not directly disturbed during read, thereby improving Read Static Noise Margin (RSNM).

7. **External RBL Precharge Circuit** : An external PMOS precharge transistor is connected to RBL in the Cadence testbench. This transistor is not part of the core 9T cell count; it is a testbench support element that precharges RBL to VDD before the read interval, then disconnects to allow the read path to determine the bit line response. Without this precharge support, the read simulation would not realistically reflect bit line behaviour.

V. Design and Analysis of 6T SRAM Cell

Technology & Supply

Parameter	Value
Technology Node	45 nm CMOS
Supply Voltage (VDD)	1.8 V
Library	gpd045 (45 nm)

The conventional 6T SRAM cell was implemented and simulated using 45 nm CMOS technology models within the Cadence Virtuoso environment. The primary objective of this implementation is to provide a functional validation of the 6T architecture, specifically evaluating its write, read and hold operations and analyzing the leakage current and read disturbance behavior during hold and read operations.

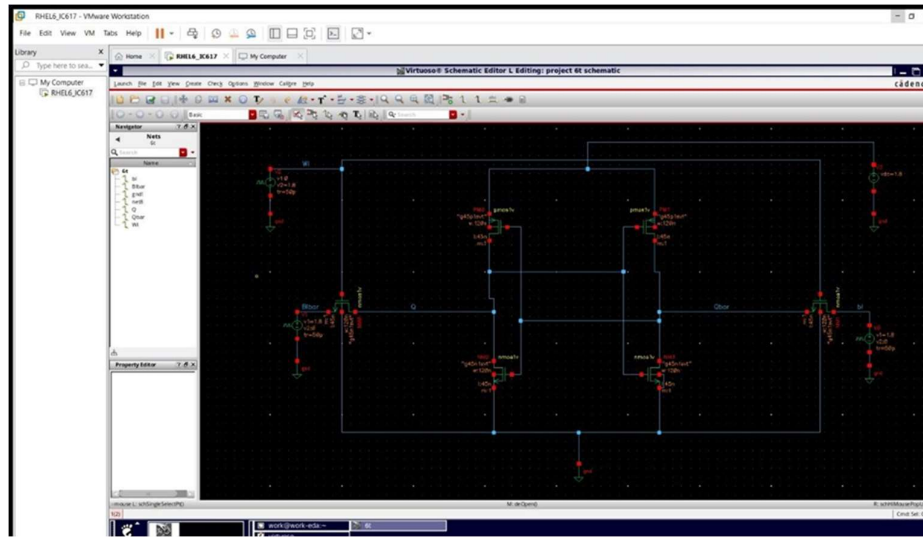


Figure 5.1: Schematic of 6T SRAM Cell

The 6T SRAM cell consists of five key signals and nodes. The Word Line (WL) is a pulse signal that switches from 0 V to 1.8 V to enable read and write operations by activating the access transistors. BL and BL bar serve as the Bit Line and Complementary Bit Line respectively, where BL is connected to the right side and BL bar to the left side of the cell for data transfer during read and write operations. Q and QB are the internal complementary storage nodes of the cross-coupled latch, where Q holds the stored data value and QB maintains its logical complement, together ensuring stable data retention during the hold operation.

Transistor parameter:

Transistor	Type	Width (W)	Length (L)	Multiplier (m)
PM1	PMOS (pmos1v)	120 nm	45 nm	1
PM2	PMOS (pmos1v)	120 nm	45 nm	1
NM1	NMOS (nmos1v)	120 nm	45 nm	1
NM2	NMOS (nmos1v)	120 nm	45 nm	1
Access Tx (left)	NMOS (nmos1v)	120 nm	45 nm	1
Access Tx (right)	NMOS (nmos1v)	120 nm	45 nm	1

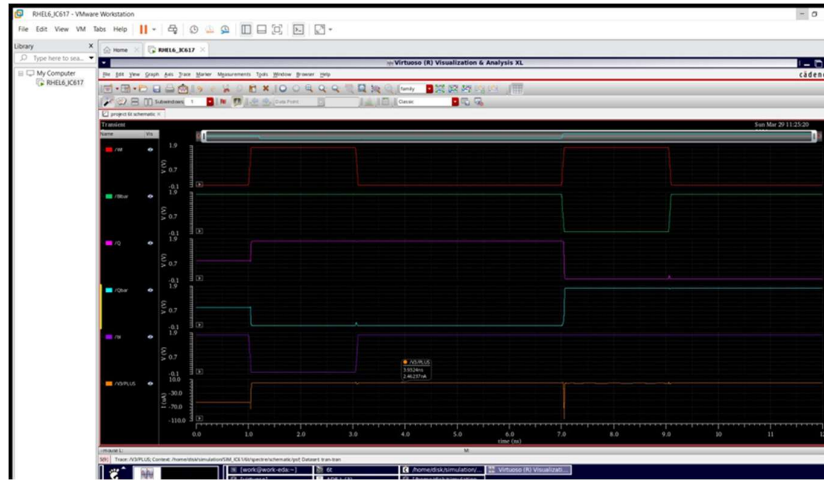


Figure 5.2 : Waveform of 6T SRAM Cell



Figure 5.3 : Leakage current waveform of 6T SRAM Cell

5.1 Transient Analysis of 6T SRAM during read and write Operations

- Initial Condition (0–1 ns) WL = 0, BL = BLbar = 1, and Q/QB start at 0 V. This represents the pre-access idle state where the cell is unpowered and the latch has not yet been initialized.
- Write-1 Operation (1–3 ns): When WL = 1, the access transistors connect the bit lines to the storage nodes. With BL = 1 and BL̄ = 0, node Q is driven to logic '1' and QB to '0' through latch feedback. A transient current spike is observed due to switching activity.
- Hold-1 Operation (3–7 ns): When WL = 0, the cell is isolated from the bit lines. The cross-coupled inverters maintain Q = 1 and QB = 0, confirming stable data retention with minimal leakage current.

- Write-0 Operation (7–10 ns): When $WL = 1$, with $BL = 0$ and $BL^- = 1$, node Q is pulled down to '0' and QB rises to VDD. The latch quickly stabilizes the new state, accompanied by transient current variations.
- Hold-0 Operation (10–12 ns): When $WL = 0$, the cell retains $Q = 0$ and $QB = 1$. The supply current settles near zero, indicating low leakage and stable storage.

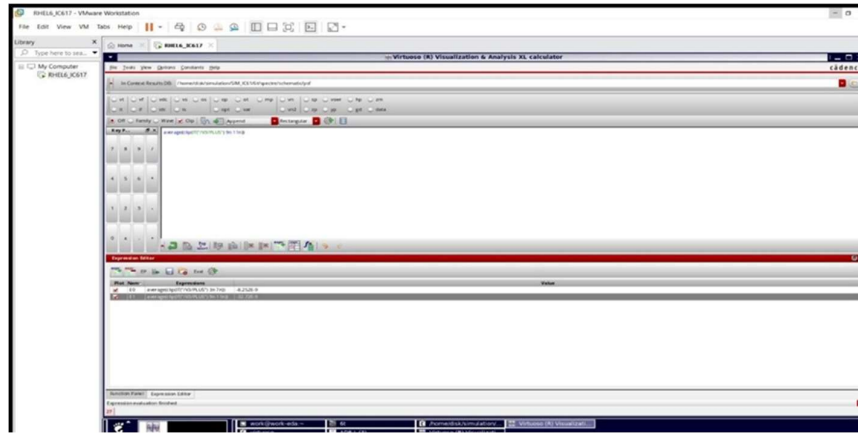


Figure 5.1.1 : Leakage current calculation for storing 0 and 1

Leakage Power Formula:

$$P_{\text{leakage}} = I_{\text{leakage}} \times VDD$$

- For Storing '1' (Hold-1 State): $P_{\text{leakage}} = -8.252 \times 10^{-9} \times 1.8 \text{ V}$

$$P_{\text{leakage}} = -14.85 \text{ nW}$$

- For Storing '0' (Hold-0 State): $P_{\text{leakage}} = -32.72 \times 10^{-9} \times 1.8 \text{ V}$

$$P_{\text{leakage}} = -58.89 \text{ nW}$$

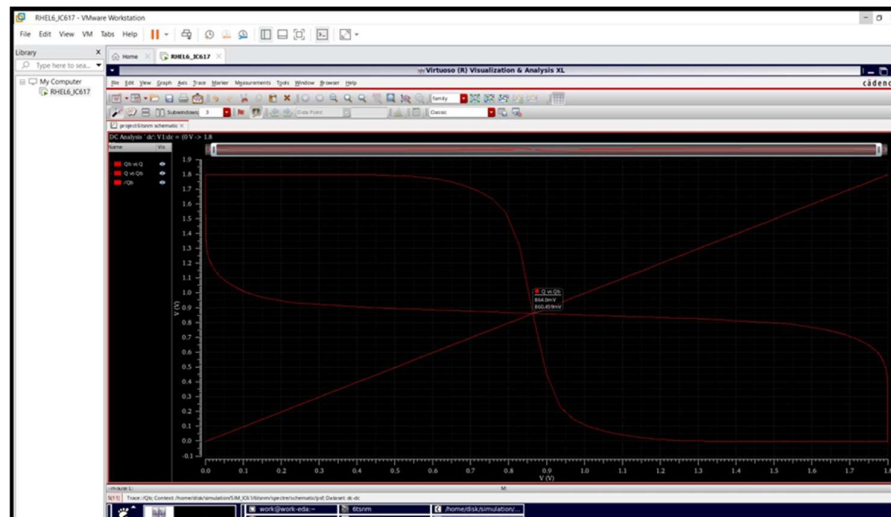


Figure 5.1.2 : butterfly curve for 6t SRAM Cell

The stability of the proposed SRAM cell is evaluated using the butterfly curve, which is obtained from the voltage transfer characteristics (VTC) of two cross-coupled inverters. The butterfly curve is generated by plotting the output voltage of one inverter against the input voltage of the other inverter and mirroring one of the characteristics along the diagonal axis.

The resulting plot forms a butterfly-shaped structure, where the two lobes represent the stable operating regions of the SRAM cell. The intersection point of the two curves corresponds to the metastable point, where both internal storage nodes (Q and $\bar{Q}$) attain nearly equal voltages. In this work, the metastable point is observed at approximately 0.864 V and 0.860 V, indicating a well-balanced inverter pair.

6. Simulation of Dynamic sleep controlled 9T SRAM Cell

In the simulated circuit, the design parameters include:

- Technology node: 45nm CMOS
- Supply voltage (VDD): 1V
- Transistor sizing (W/L): to ensure read and write stability, reduce leakage, drive strength of pull-up and pull down transistor.
- Design Parameters: cross- coupled storage latch, single-ended write path, power- gated write support through WLPD, leakage balancing transistor(mad),pmos based read-path, external rbl precharge pmos transistor.

The PMOS-Reading 9T (PR9T) SRAM cell was implemented and simulated using 45 nm CMOS technology models within the Cadence Virtuoso environment. The primary objective of this implementation is to provide a functional validation of the PR9T architecture, specifically evaluating its write, read and hold operation and analyzing leakage current during hold operation.

The implemented schematic consists of :

- the cross-coupled latch that stores the logic state.
- the single-ended write path connected through WBL.
- the separate PMOS-based read path connected through RBL.

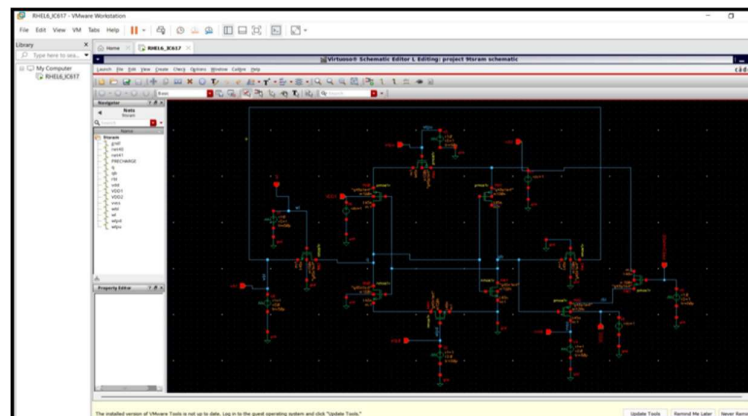


Figure 6.1 : schematic of PR9T SRAM cell

The schematic consist of 9 transistor along with one test bench precharge pmos used for charging rbl. The core of cell is a cross coupled storage latch formed by connecting two back-to-back CMOS inverter, which generates complementary internal nodes Q and QB this nodes stores the data. A single ended write Bitline is employed to reduce dynamic swithching activity. Power gating technique is used to drive WLPD and WLPD ,their function is to improve the write stability of the cell by reducing the resistance offered by the cross coupled inverters when new data is forced into the storage node. Another defining feature of the PR9T architecture is the MDR transistor, which acts as a leakage-balancing element. The PMOS-based read path reduces leakage in the read operation, thereby improving the stability of the SRAM cell. An additional PMOS transistor, referred to as the external RBL precharge PMOS, is connected to the read bitline (RBL). This transistor is driven by a separate control signal and is used exclusively as a precharge device during transient simulations.

It should be noted that this PMOS transistor is not part of the core 9T SRAM cell. Instead, it serves as a testbench support element to ensure proper evaluation of the read bitline waveform in Cadence simulations.



Figure 6.2 : Waveform of PR9T SRAM Cell



Figure 6.3 : leakage current waveform of the PR9T SRAM Cell

6.1 Transient Analysis of PR9T SRAM Cell Operations

- Initial condition (0-4 ns) : WL = 0, WBL = 1, and Q/QB start at intermediate voltages while RBL remains high. This represents an uninitialized state where the latch has not yet settled. Such behavior is typical in transient simulations without predefined initial conditions.

- Write-1 operation (4-8 ns) : WL = 1, WBL = 1 $\rightarrow$ Q rises to '1' and QB falls to '0'. The NMOS access transistor connects WBL to Q, forcing it high, while latch feedback pulls QB low. The gradual rise of Q is expected due to weak '1' transmission through NMOS and internal capacitance effects.

- Hold-1 (8-12 ns) : WL = 0 $\rightarrow$ Q = 1, QB = 0 remain stable; RBL stays high. This confirms proper data retention via cross-coupled latch feedback after write disconnection.

- Read-1 (12-18 ns) : Stored state: Q = 1, QB = 0 $\rightarrow$ RBL discharges. Since QB = 0, the PMOS read transistor turns ON, pulling RBL down. This verifies correct and non-destructive read operation in the decoupled PR9T read path.

- Bit line transition (16-20 ns) : WBL switches to 0 while WL = 0 $\rightarrow$ no change in Q/QB. This confirms that data is not disturbed without WL activation, ensuring write stability.

- Write-0 (20-24 ns) : WL = 1, WBL = 0 $\rightarrow$ Q drops to '0', QB rises to '1'. The transition is faster due to strong '0' passing through NMOS. Latch feedback quickly stabilizes the new state.

- Hold-0 (24-28 ns) : WL = 0 $\rightarrow$ Q = 0, QB = 1 remain stable; RBL stays high. This confirms reliable storage of logic '0'.

- Read-0 (~28 ns) : Stored state: Q = 0, QB = 1 $\rightarrow$ RBL remains high with slight disturbance. The PMOS read path is OFF, preventing discharge. Minor glitches are due to parasitic and coupling effects, not functional errors.

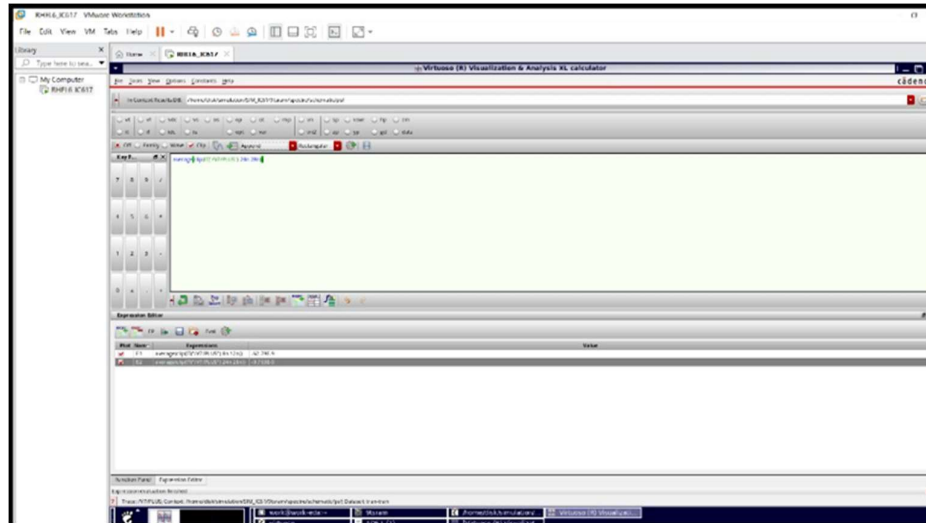


Figure 6.1.1 : leakage current calculation for storing 0 and 1

6.2 Leakage Power Formula

- P leakage : Leakage Power (watts)
- I leakage : Leakage Current (Amperes)
- VDD : Supply Voltage (volts)

$$P_{\text{leakage}} = I_{\text{leakage}} \times V_{\text{dd}}$$

$$P_{\text{leakage}} = -62.79 \times 10^{-9} \times 1 \text{ V (for storing 0)}$$

$$P_{\text{leakage}} = -62.79 \times 10^{-9} \text{ W}$$

$$P_{\text{leakage}} = -9.703 \times 10^{-9} \times 1 \text{ V (for storing 1)}$$

$$P_{\text{leakage}} = -9.703 \times 10^{-9} \text{ W}$$

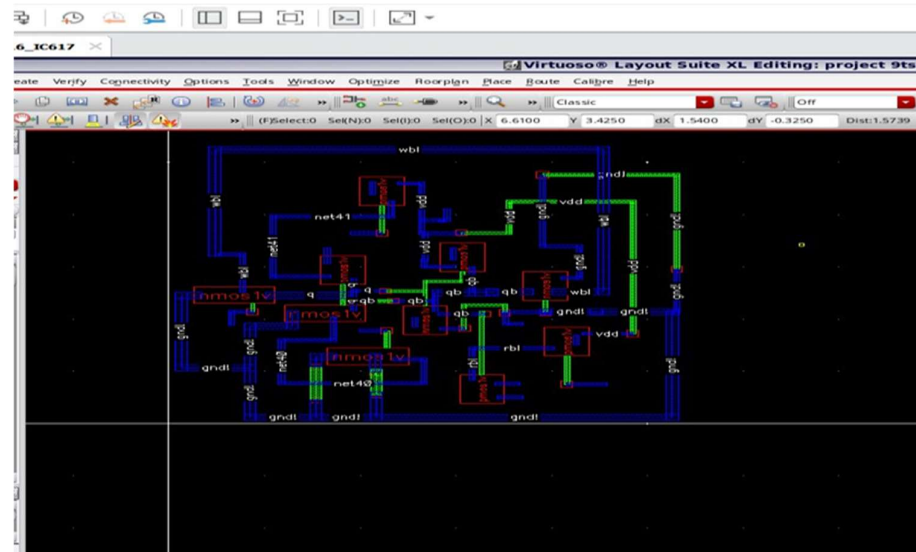


Figure 6.2.1 : Layout of PR9T SRAM Cell

Conclusion and future work:

The PR9T SRAM cell was successfully implemented and verified in 45 nm Cadence technology, incorporating key features such as a single-ended write path, power-gated write support, and a decoupled read path for improved leakage and power balance. Transient analysis confirmed correct read, write, and hold operations, and the layout design validated its suitability for VLSI implementation. Future work will focus on post-layout simulations and PVT variation analysis.

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